

# FDC3616N

## 100V N-Channel PowerTrench® MOSFET

### General Description

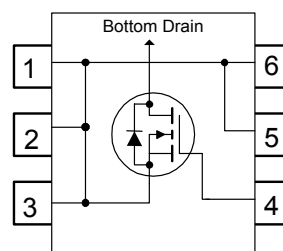
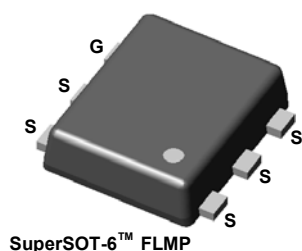
This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low  $R_{DS(ON)}$  and fast switching speed.

### Applications

- DC/DC converter
- Load Switching

### Features

- 3.7 A, 100 V.  $R_{DS(ON)} = 70\text{ m}\Omega @ V_{GS} = 10\text{ V}$   
 $R_{DS(ON)} = 80\text{ m}\Omega @ V_{GS} = 6.0\text{ V}$
- High performance trench technology for extremely low  $R_{DS(ON)}$
- Low gate charge (23nC typical)
- High power and current handling capability
- Fast switching speed.



### Absolute Maximum Ratings T<sub>A</sub>=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain-Source Voltage	100	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Drain Current – Continuous (Note 1a)	3.7	A
	– Pulsed	20	
$P_D$	Maximum Power Dissipation (Note 1a) (Note 1b)	2	W
		1.1	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a) (Note 1b)	60	°C/W
		111	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.5	

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
.616	FDC3616N	7"	8mm	3000 units

**Electrical Characteristics** $T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Drain-Source Avalanche Ratings** (Note 2)

$W_{DSS}$	Drain-Source Avalanche Energy	Single Pulse, $V_{DD} = 50\text{ V}$ , $I_D = 3.7\text{ A}$			244	mJ
$I_{AR}$	Drain-Source Avalanche Current				3.7	A

**Off Characteristics**

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}$ , $I_D = 250\ \mu\text{A}$	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		114		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 80\text{ V}$ , $V_{GS} = 0\text{ V}$			10	$\mu\text{A}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 30\text{ V}$ , $V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage, Forward	$V_{GS} = 20\text{ V}$ , $V_{DS} = 0\text{ V}$			100	nA
$I_{GSSR}$	Gate-Body Leakage, Reverse	$V_{GS} = -20\text{ V}$ , $V_{DS} = 0\text{ V}$			-100	nA

**On Characteristics** (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 250\ \mu\text{A}$	2	2.5	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		-7.4		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On Resistance	$V_{GS} = 10\text{ V}$ , $I_D = 3.7\text{ A}$ $V_{GS} = 6.0\text{ V}$ , $I_D = 3.5\text{ A}$ $V_{GS} = 10\text{ V}$ , $I_D = 3.7\text{ A}$ , $T_J = 125^\circ\text{C}$		55 58 104	70 80 139	m $\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{ V}$ , $I_D = 3.7\text{ A}$		19		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 50\text{ V}$ , $V_{GS} = 0\text{ V}$ ,		1215		pF
$C_{oss}$	Output Capacitance	$f = 1.0\text{ MHz}$		72		pF
$C_{rss}$	Reverse Transfer Capacitance			39		pF
$R_G$	Gate Resistance	$V_{GS} = 15\text{ mV}$ , $f = 1.0\text{ MHz}$		1.1		$\Omega$

**Switching Characteristics** (Note 2)

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\text{ V}$ , $I_D = 1\text{ A}$ ,		9	18	ns
$t_r$	Turn-On Rise Time	$V_{GS} = 10\text{ V}$ , $R_{GEN} = 6\ \Omega$		4	8	ns
$t_{d(off)}$	Turn-Off Delay Time			28	45	ns
$t_f$	Turn-Off Fall Time			10	20	ns
$Q_g$	Total Gate Charge	$V_{DS} = 50\text{ V}$ , $I_D = 3.7\text{ A}$ ,		23	32	nC
$Q_{gs}$	Gate-Source Charge	$V_{GS} = 10\text{ V}$		4.8		nC
$Q_{gd}$	Gate-Drain Charge			5.4		nC

## Electrical Characteristics

$T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Drain–Source Diode Characteristics and Maximum Ratings</b>						
$t_{rr}$	Diode Reverse Recovery Time	$I_F = 3.7\text{ A}$ ,		41		nS
$Q_{rr}$	Diode Reverse Recovery Charge	$d_{IF}/d_t = 100\text{ A}/\mu\text{s}$		107		nC
$I_S$	Maximum Continuous Drain–Source Diode Forward Current				2.1	A
$V_{SD}$	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = 2.1\text{ A}$ (Note 2)		0.75	1.2	V

**Notes:**

1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



- a)  $60^\circ\text{C}/\text{W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper



- b)  $111^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width <  $300\mu\text{s}$ , Duty Cycle < 2.0%

## Typical Characteristics

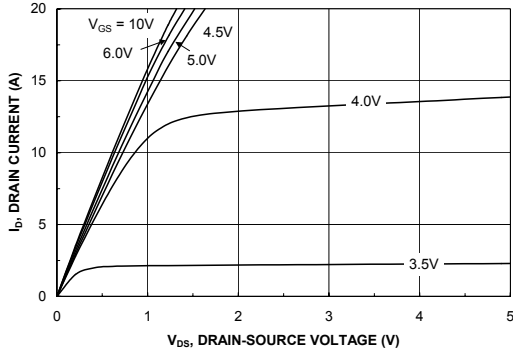


Figure 1. On-Region Characteristics.

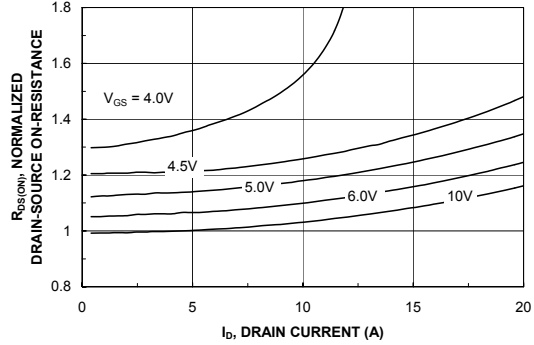


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

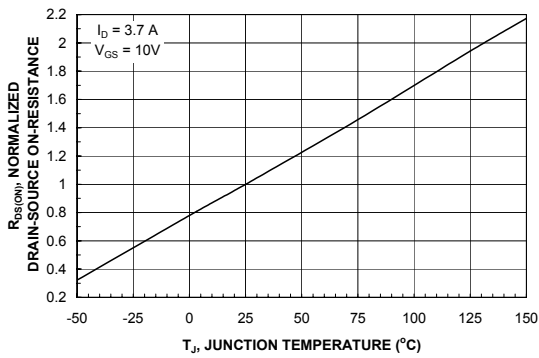


Figure 3. On-Resistance Variation with Temperature.

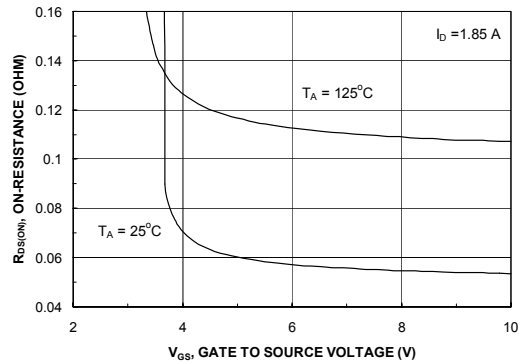


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

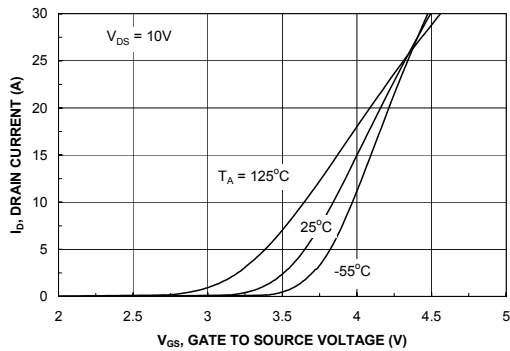


Figure 5. Transfer Characteristics.

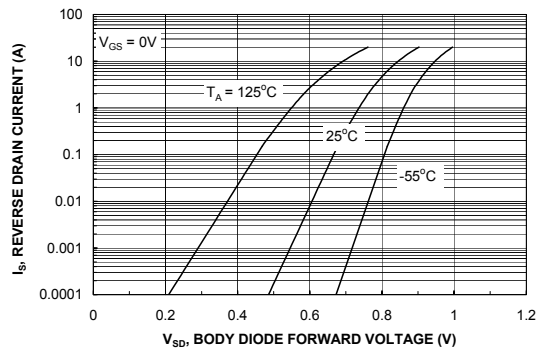


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

## Typical Characteristics

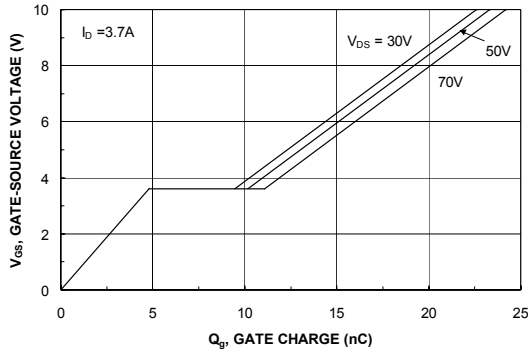


Figure 7. Gate Charge Characteristics.

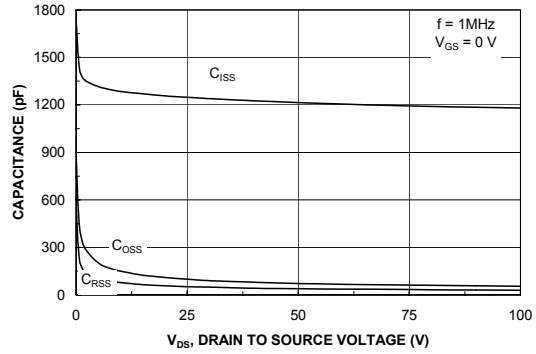


Figure 8. Capacitance Characteristics.

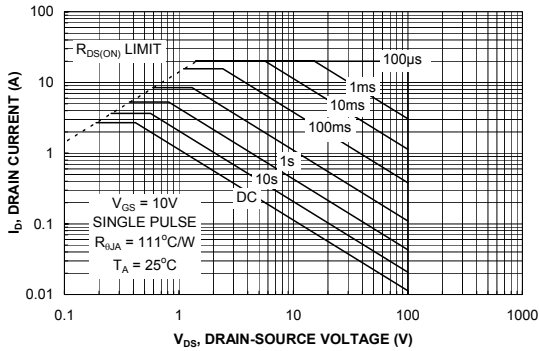


Figure 9. Maximum Safe Operating Area.

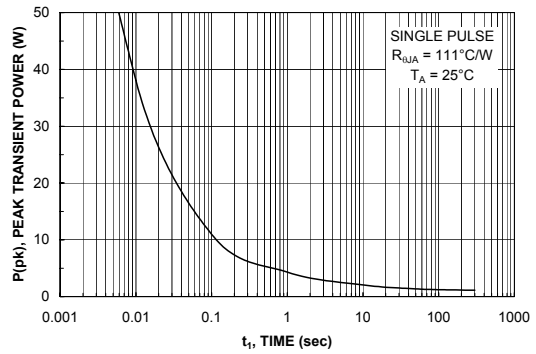


Figure 10. Single Pulse Maximum Power Dissipation.

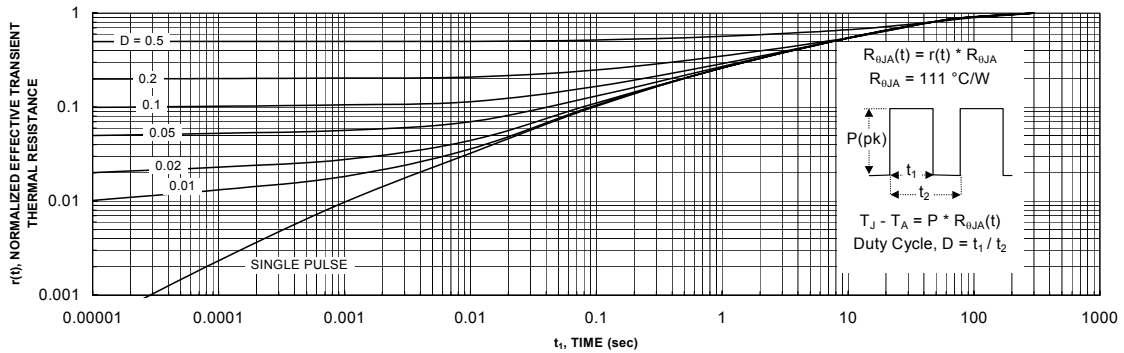
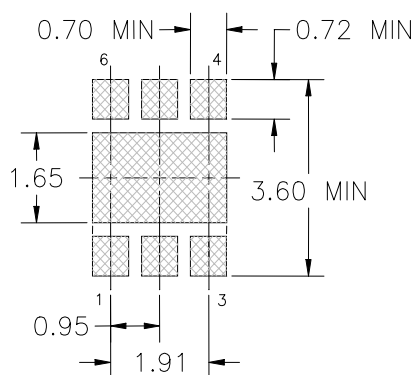
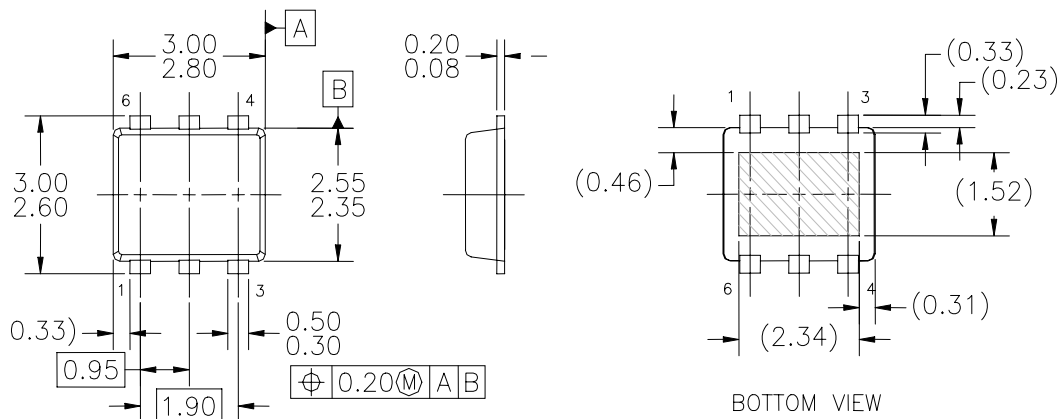


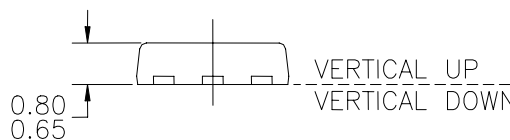
Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.  
Transient thermal response will change depending on the circuit board design.

### Dimensional Outline and Pad Layout



LAND PATTERN  
RECOMMENDATION



NOTES: UNLESS OTHERWISE SPECIFIED

- A) NO PACKAGE STANDARD REFERENCE AS OF MARCH, 2001.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH AND CUTTING BURRS.
- D) LEAD TIP BURR:  
 HORIZONTAL: 0.20 mm MAX  
 VERTICAL UP: 0.20 mm MAX  
 VERTICAL DOWN: 0.05 mm MAX

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CoolFET™	FPST™	MicroFET™	QFET®	SuperSOT™-8
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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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